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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/802,584	03/08/2001	Shekhar Y. Borkar	10559/412001 / P10349	7790

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EXAMINER	
COX, CASSANDRA F	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 04/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/802,584	Applicant(s) BORKAR ET AL.	
	Examiner Cassandra Cox	Art Unit 2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *05/21/001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicant's arguments filed 1/18/02 have been fully considered but they are not persuasive. Therefore, the previous rejections are repeated below.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 5-6, 9, 12, 14-15, 17, and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawabata et al. (U. S. Patent No. 5,936,912).

In reference to claim 1, Kawabata discloses in Figure 4, a device comprising a delay lock loop circuit (15, 16, 17, 18, 19) responsive to an input signal (E-CLK) to delay the input signal (E-CLK) by a first period; and a delay circuit (14) coupled to the delay lock loop circuit (15, 16, 17, 18, 19) and responsive to the input signal (E-CLK), the delay circuit 914) being responsive to a control signal from the delay lock loop circuit (15, 16, 17, 18, 19; column 5, lines 17-20) to delay the input signal (E-CLK) by a second period. The same applies to claims 9, 14 and 17 wherein the first input signal is seen to be the output of the frequency divider (15).

In reference to claim 5, Kawabata discloses in Figure 5, that the delay lock loop (15, 16, 17, 18, 19) circuit further comprises at least one delay cell (24n, 25n, 23n); and in Figure 4 a phase detector (18) responsive to the input signal (E-CLK) and responsive to an output signal (D-CLK) from the at least one delay cell (24n, 25n, 23n) to produce a

control signal (column 5, lines 13-20). The same applies to claims 6, 12, 15, and 19-20 (see column 4, line 66- column 5, line 2).

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Taniguchi et al. (U.S. Patent No. 6,225,843).

In reference to claim 1, Taniguchi discloses in Figure 1 a device comprising a delay lock loop circuit responsive to an input signal (CLK) to delay the input signal (CLK) by a first period; and a delay circuit (154) coupled to the delay lock loop circuit and responsive to the input signal (/CLK), the delay circuit being responsive to a control signal from the delay lock loop circuit to delay the input signal by a second period (column 1, lines 59-62). The same applies to claims 9 and 14.

In reference to claim 2, Taniguchi discloses in column 4, lines 25-28 that in input signal (CLK, /CLK) comprises complementary clock signals. The same applies to claims 10 and 17.

In reference to claim 3, Taniguchi discloses in column 1, lines 55-60 that the delay circuit (154) and the delay line (155) used in the delay lock loop circuit are constructed in the same manner and would therefore have substantially the same period since they are both controlled by the phase error signal from the delay lock circuit. The same applies to claim 19.

In reference to claim 4, Taniguchi discloses in Figure 1 a first input channel (151) coupled to the delay lock loop circuit and a second input channel (150) coupled to the delay circuit (154).

In reference to claim 5, Taniguchi discloses in Figure 4A the at least one delay cell (401, 402, 403); and in Figure 1, a phase detector (157) responsive to the input signal (CLK) and responsive to an output signal from the at least one delay cell (401, 402, 403; which is seen to be a delay cell contained in delay line 155) to produce a control signal. The same applies to claims 6, 12-13, 15, and 20.

In reference to claim 7, Taniguchi further discloses in Figure 1 a latch circuit (162) having a first input to receive an input data signal (DATA) and a second input to receive one of an output (/CLK1) from the delay circuit and an output (CLK1) from the delay lock loop circuit. The same applies to claims 11 and 16.

In reference to claim 8, Taniguchi discloses in Figure 4C a delay line, used in the delay lock loop circuit, that comprises a center tap (which is seen as the output of inverter 403-2).

In reference to claim 18, Taniguchi discloses in Figure 1, that the first and second input signals are clock signals (CLK, /CLK) and that the method of operating the latch circuit (162) comprises activating the latch on a rising edge of one of the first delayed clock signal (CLK1) and the second delayed clock signal (/CLK1) (see column 1, line 65- column 2, line 1).

Response to Arguments

4. Applicant's arguments filed 01/18/02 have been fully considered but they are not persuasive. Applicant argues that the prior art of record fails to disclose a circuit wherein one or more of the delay lines is responsive to a control signal from the other delay line. The examiner points out, however, that this limitation is not stated in the claims.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 703-306-5735. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (703)-308-4876. The fax phone

numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

CC
CC
April 19, 2002

Kenneth B. Wells
Primary Examiner